IN THE CLAIMS

Claims 1-14 (Canceled)

Claim 15 (previously amended): A high performance buffering technique for use with a serial peripheral interface to facilitate high data rates, said buffering technique comprising the steps of

initializing a single buffer to act as transmitter and receiver by writing data to a data register;

performing a transmit buffering sequence to prepare for the transmitting of the data;

performing a transmit and receive shifting sequence to facilitate transmitting of the data and receiving of new data at substantially the same time; and

performing a receive buffering sequence to prepare for the receipt of additional new data.

Claim 16 (original): The high performance buffering technique of claim 15, wherein said initialization step comprises the step of:

writing the data into a location of said buffer as designated by a write pointer.

Claim 17 (previously amended): The high performance buffering technique the steps of:

incrementing of claim 15, wherein said transmit buffering sequence comprises a write pointer to prevent a next byte to be transmitted from overwriting a previous written byte; and

incrementing a write shift counter to facilitate tracking of a number of bytes available for transmission.

Claim 18 (canceled)

Claim 19 (previously amended): The high performance buffering technique of claim 15, wherein said receive buffering sequence comprises the steps of:

incrementing a shift pointer to identify a new location in the buffer for receiving data; and

incrementing a read shift counter to indicate that the new data has been received.

Claim 20 (original): The high performance buffering technique of claim 15, wherein said buffering technique further comprises the steps of:

interrupting a CPU if the data is ready for transmitting and said buffer is approximately full; and

interrupting the CPU if said buffer is ready to receive data and said buffer is approximately empty.

REMARKS

Claims 15-20 are pending in the application. Claims 15-20 are rejected. Claim 18 has been cancelled.

Claims 15-17, 19, and 20 were rejected under 35 USC 103(a) as being unpatentable over Thomsen in view of Yasoshima. Claim 15 includes ... initializing a single buffer to act as transmitter and receiver by writing data to a data register; ... performing a transmit and receive shifting sequence to facilitate transmitting of the data and receiving of new data at substantially the same time ... . The references of record do not show, teach, or suggest the above recited limitations of claim 15. The Yasoshima reference does not disclose a single buffer to facilitate transmitting and receiving at substantially the same time. The references do not teach how the device of Yasoshima can be combined with Thomsen to obtain a single buffer for performing a transmit and receive shifting sequence to facilitate transmitting of the data and receiving of new data. Claims 16, 17, 19, and 20 depend from claim 15. Therefore, claims 15-17, 19, and 20 are believed to be allowable over the references of record.